No Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-16 (Canceled)

17. (Original) A circuit for remapping a specific row address bit to a specific column address bit, comprising:

a first latch coupled to receive the specific row address bit, the latch being operable to store the specific row address bit responsive to a row address strobe signal and to then output the stored row address bit;

a second latch coupled to receive a first set of column address bits and the specific column address bit, the latch being operable to store the first set of column address bits and the specific column address bit responsive to a column address strobe signal and to then output the stored column address bits, including the specific column address bit; and

a selector operable to select either the specific row address bit output from the first latch or the specific column address bit output from the second latch, the selected address bit being combined with the column address bits in the first set.

18. (Original) The remapping circuit of claim 17 wherein the selector comprises:

a first pass gate coupled between an output of the first latch and an address output terminal;

a second pass gate coupled between an output of the second latch and the address output terminal; and

a control circuit for enabling the first pass gate and disabling the second pass gate or disabling the first pass gate and enabling the second pass gate.

Claims 19-29 (Canceled)

30. (Original) A dynamic random access memory ("DRAM") comprising:

an array of memory cells arranged in rows and columns;

a circuit for remapping a specific row address bit to a specific column address bit, comprising:

a remapping latch coupled to receive the specific row address bit, the remapping latch being operable to store the specific row address bit responsive to a row address strobe signal and to then output the stored row address bit;

a column address latch coupled to receive a first set of column address bits and the specific column address bit, the column address latch being operable to store the first set of column address bits and the specific column address bit responsive to a column address strobe signal and to then output the stored column address bits, including the specific column address bit; and

a selector operable to select either the specific row address bit output from the remapping latch in a reduced density mode or the specific column address bit output from the column address latch in a full density mode, the selected address bit being combined with the column address bits in the first set to provide a composite column address;

a column decoder coupled to the selector to receive the composite column address and enable respective sense amplifiers corresponding thereto;

a row address latch structured to store a row address responsive to a row address strobe signal;

a first row decoder coupled to the row address latch to receive the stored row address and activate respective word lines corresponding thereto, the first row decoder being enable responsive to a first enable signal;

a second row decoder coupled to the row address latch to receive the stored row address and activate respective word lines corresponding thereto, the row lines activated by the first row decoder being interleaved with the row lines activated by the second row decoder, the second row decoder being enabled responsive to a second enable signal;

a mode controller coupled to the row decoders, the mode controller being operable in the full density mode to generate the first enable signal responsive to a first state of a

least significant bit of the row address and to generate the second enable signal responsive to a second state of the least significant bit of the row address, the mode controller further being operable to generate the first and second enable signals in the reduced density mode regardless of the state of the least significant bit of the row address; and

a data path coupled between the memory array and a data terminal.

31. (Previously Presented) The dynamic random access memory of claim 30 wherein the selector comprises:

a first pass gate coupled between an output of the column address latch and an address output terminal;

a second pass gate coupled between an output of the remapping latch and the address output terminal; and

a control circuit for enabling the first pass gate and disabling the second pass gate or disabling the first pass gate and enabling the second pass gate.

Claims 32-38 (Canceled)

39. (Original) A computer system, comprising:

a data input device;

a data output device;

a processor coupled to the data input and output devices; and

a dynamic random access memory, comprising:

an array of memory cells arranged in rows and columns;

a circuit for remapping a specific row address bit to a specific column address bit, comprising:

a remapping latch coupled to receive the specific row address bit, the remapping latch being operable to store the specific row address bit responsive to a row address strobe signal and to then output the stored row address bit;

a column address latch coupled to receive a first set of column address bits and the specific column address bit, the column address latch being operable to store the first set of column address bits and the specific column address bit

responsive to a column address strobe signal and to then output the stored column address bits, including the specific column address bit; and

a selector operable to select either the specific row address bit output from the remapping latch in a reduced density mode or the specific column address bit output from the column address latch in a full density mode, the selected address bit being combined with the column address bits in the first set to provide a composite column address;

a column decoder coupled to the selector to receive the composite column address and enable respective sense amplifiers corresponding thereto;

a row address latch structured to store a row address responsive to a row address strobe signal;

a first row decoder coupled to the row address latch to receive the stored row address and activate respective word lines corresponding thereto, the first row decoder being enable responsive to a first enable signal;

a second row decoder coupled to the row address latch to receive the stored row address and activate respective word lines corresponding thereto, the row lines activated by the first row decoder being interleaved with the row lines activated by the second row decoder, the second row decoder being enabled responsive to a second enable signal;

a mode controller coupled to the row decoders, the mode controller being operable in the full density mode to generate the first enable signal responsive to a first state of a least significant bit of the row address and to generate the second enable signal responsive to a second state of the least significant bit of the row address, the mode controller further being operable to generate the first and second enable signals in the reduced density mode regardless of the state of the least significant bit of the row address; and

a data path coupled between the memory array and a data terminal.

40. (Previously Presented) The computer system of claim 39 wherein the selector comprises:

a first pass gate coupled between an output of the column address latch and an address output terminal;

a second pass gate coupled between an output of the remapping latch and the address output terminal; and

a control circuit for enabling the first pass gate and disabling the second pass gate or disabling the first pass gate and enabling the second pass gate.

Claims 41-43 (Canceled)

44. (Previously Presented) A method of addressing a dynamic random access memory ("DRAM") having a full density operating mode and a reduced density operating mode, the method comprising:

determining the operating mode of the DRAM;

storing a specific row address bit responsive to a row address strobe signal;

storing a first set of column address bits and a specific column address bit responsive to a column address strobe signal; and

in the full density operating mode, selecting the first set of column address bits and the specific column address bit that were stored responsive to the column address strobe signal;

in the reduced density operating mode, selecting the first set of column address bits that were stored responsive to the column address strobe signal and the specific row address bit that was stored responsive to the row address strobe signal; and

addressing a column of the DRAM using the selected address bits.

45. (Original) The method of claim 44, further comprising addressing a row of the DRAM, the method comprising:

storing a second set of row address bits along with the specific row address bit responsive to the row address strobe signal; and

addressing a row of the DRAM using the stored second set of row address bits.

Claims 46-47 (Canceled)